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Final Report

on

FUNDAMENTAL STUDIES AND DEVICE DEVELOPMENT IN BETA SILICON CARBIDE

Supported by ONR Under Contract N00014-82-K-0182P0005

For the Period February 1, 1985 – January 31, 1988

School of Engineering

North Carolina State University

Raleigh, North Carolina

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SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER 243-043-00012	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) Fundamental Studies and Device Development in Beta Silicon Carbide		5. TYPE OF REPORT & PERIOD COVERED Final Report 2/1/85 - 1/31/88 6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) Robert F. Davis		8. CONTRACT OR GRANT NUMBER(s) N00014-82-K-0182 P0005
9. PERFORMING ORGANIZATION NAME AND ADDRESS North Carolina State University Dept. of Materials Engineering Box 7907, Raleigh, NC 27695-7907		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS PE 61153N RR 021-02-03 NR 243-027
11. CONTROLLING OFFICE NAME AND ADDRESS ONR-414 Arlington, VA 22217		12. REPORT DATE 3/30/88 13. NUMBER OF PAGES
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)		15. SECURITY CLASS. (of this report) Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

ONR Scientific Officer; Tel: (202) 696-4218

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Silicon Carbide	Dry etching	p-n junctions
Chemical vapor deposition	electron microscopy	
electronic materials	electrical properties	
in situ doping	ohmic contacts	
ion implantation	field effect transistor	

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The research of this three year reporting period has involved (1) the CVD of β-SiC on off-axis Si (100), (2) the growth of β- and α-SiC on monocrystalline α-SiC substrates, (3) high temperature ion implantation, and damage production studies (4) the continued development and characterization of ohmic and rectifying contacts for n- and p-type SiC, (5) reactive ion and plasma etching, and (6) the fabrication and evaluation of p-n junctions, Schottky barrier diodes, MESFETs and MOSFETs in β-SiC.

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S/N 0102-014-6601

Enclosure (1)

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

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SUMMARY

High purity monocrystalline β-SiC films have been chemically vapor deposited on Si(100) and α-SiC(0001) at 1660K-1823K and 0.1 MPa using SiH_4 and C_2H_4 carried in H_2. Films grown on the on-axis Si(100) contained substantial concentrations of dislocations, stacking faults and antiphase boundaries; those deposited on α-SiC(0001) contained primarily double positioning boundaries. These boundaries were eliminated by using off-axis orientations of the respective substrates. Films produced on Si(100) have also been doped during growth and via ion implantation with B or Al (p-type) or P or N (n-type) at liquid nitrogen, room and elevated temperatures. Results from the former procedure showed the ionized dopant/total dopant concentration ratios for N, P, B and Al to be 0.1, 0.2, 0.002 and 0.01, respectively. The solubility limits of N, P and B at 1660K were determined to be ~ 2E20, 1E18 and 8E18 cm^{-3}, respectively; that of Al exceeds 2E19 cm^{-3}. High temperature ion implantation coupled with dynamic and post annealing resulted in a markedly reduced defect and precipitate concentration relative to that observed in similar research at the lower temperatures. Dry etching in CF_4 and NF_3 by reactive ion etching (RIE) and in SF_6 by plasma etching have also been conducted. Device-compatible surface impurity chemistry and morphology were only obtained using RIE and NF_3 combined with a C cathode. Schottky diode, p-n junctions, MESFET and MOSFET devices have been fabricated. The p-n junctions have the characteristics of insulators containing injected carriers. The current-voltage characteristics of the MESFETs measured from 298 to 623K indicated reasonable

performance throughout this range. The maximum tranconductance was 1.6 mS/mm; the value of this parameter decreased with temperature. Similar data were obtained on both enhancement mode and depletion mode MOSFETs; the latter operated contiuously as high as 923K. Transconductances as high as 11.90 mS/mm were achieved.

1 INTRODUCTION

Silicon carbide is the only compound species that exists in the solid state in the Si-C system, but it can occur in many polytype structures [1]. The lone cubic polytype crystallizes in the zinc blende structure and is denoted as ß-SiC. The ~ 170 known additional hexagonal and rhombohedral polytypes are collectively referred to as α-SiC. The electron Hall mobility of high-purity undoped ß-SiC has been postulated from theoretical calculations to be greater than that of the α forms over the temperature range of 300-1000K because of the smaller amount of phonon scattering in the cubic material [2]. Although this result has served as one catalyst for the current international interest in ß-SiC, this material also possesses a unique combination of additional properties including a high melting point (3103K at 30 atm) [3], high thermal conductivity (3.9 W/cm•deg) [4]. wide band gap (2.2 eV at 300K) [5], high breakdown electric field (2.5×10^6 V/cm) [6], high saturated drift velocity (2×10^7 m/s) [7] and small dielectric constant (9.7) [8]. As such, ß-SiC has been theoretically shown [9] to be superior to Si, GaAs or InP using either Johnson's [10] or Keyes' [11] figure of merit for high-frequency, high speed and high power transistor applications.

The high thermal conductivity and breakdown field also indicate that the integration of devices made from ß-SiC can be achieved with high densities. Two additional reasons for the renewed interest in ß-SiC are the significant advances in the growth of monocrystalline thin films of this material by chemical vapor deposition (CVD) and the ability to dope this material with n- and p-type dopants during growth or via ion implantation. As a result, devices from this material have now become a reality.

2 REVIEW OF PRIOR RESEARCH ON GROWTH, DOPING AND DEVICE DEVELOPMENT IN BETA SiC

Monocrystalline Si has been almost universally adopted as the current substrate of choice for the growth of the ß-SiC thin films because of the availability of the former in well characterized and reproducible forms of controlled purity. Amelioration of the mismatches in the coefficients of thermal expansion (~8%) and lattice parameters (~20%) via the initial reaction of the Si (100) surface with a C-containing gas followed by the successful epitaxial deposition of relatively thick (up to 30 μm), crack-free ß-SiC films on this converted layer using individual C- and Si-containing gases has been reported by Nishino et al. [8,12] and subsequently by Suzuki and co-workers [13], Addamiano and Klein [14], Sasaki et al. [15] and Liaw and Davis [16]. This two-step process is described in the following section.

Beta-SiC has also been grown on monocrystalline α-SiC substrates in the temperature range of 1773K-1973K [17, 18]. However, the growth conditions were not optimized and the interface between the various SiC epilayers and their SiC substrates was not investigated.

A limited number of studies have been conducted to investigate the incorporation via CVD techniques of electronically active impurities in ß-SiC. Bartlett et al. [19], Long et al. [20], and Nishino et al. [21] produced p-type ß-SiC by adding B_2H_6 or $AlCl_3$ during the growth of this normally n-type (unintentionally doped) material. In addition, von Muench and Pettenpaul [22] doped polycrystalline ß-SiC p-type by flowing H_2 through trimethylaluminum (TMA) during crystal growth via the van Arkel process.

As an alternative to in situ doping, diffusion and ion implantation provide means

of controllably introducing impurities into semiconductor materials. In SiC, diffusion processes require both temperatures greater than 2273K and relatively long times to accomplish the mass transport required for device fabrication. Under these conditions, masking oxide layers, essential for selective doping, vaporize and SiC decomposition occurs. Therefore, a more viable solution is ion implantation.

The Group IIIA elements of B, Al, Ga, In and Tl; the Group VA elements of N, P, Sb and Bi as well as Be have also been implanted into 6H α-SiC single crystals in research directly related to microelectronics [23-27]. Functional p-n junctions have been successfully produced [23-26] via implantation of Group VA elements into in situ doped p-type layers. By contrast, the implantation of the Group IIIA elements into n-type 6H SiC has almost always resulted in high resistivity layers but not p-type conduction [27]; the one exception is the implantation of Al reported by Kalinina et al. [28]. No implantation has been conducted in ß-SiC.

In order to electrically characterize the ß-SiC films via pn junction measurements, as well as fabricate certain devices, a method of selective, controllable etching is needed. However, SiC is an extremely inert material that can only be conventionally etched by molten salts or Cl_2 or H_2 gases at high temperatures [29]. Therefore, dry etching techniques using fluorinated gases have been investigated. Previous experiments of this type on ß-BiC thin films have all used CF_4 and $CF_4 + O_2$ mixtures in a variety of modes, including reactive ion beam etching [30], reactive ion etching [31] and plasma etching [32]. These techniques and the various parameters employed in their use did not result in etched surfaces sufficiently smooth for devices.

Good contacts are also essential for successful device fabrication in any semiconductor. Several metallic elements (e.g., W, Mo, Cr, Ni) and alloys (e.g., Au-Ta,

Au-Ta-Al, W-Mo, Cr-Ni, Cu-Ti, Al-Si) have been developed as ohmic contacts for α-SiC [33-37]; however, no information on the specific resistivities of these contacts was reported. For the majority of the contact materials note above, annealing temperatures exceeding 2000K were required to achieve ohmic character. This temperature treatment often results in deep penetration of the deposited contact material which can cause electrical shorting of devices. Moreover, the success of these contacts on hexagonal, α-SiC does not guarantee that they will be suitable for the cubic, ß form, which is of primary interest in the current study. In the case of ß-SiC, as-deposited and annealed Al have been shown [38] to be ohmic on n-type and p-type material, respectively. Again, no values of the contact resisivities were reported. Finally, in no case has the dependence of the contact resistivity on operating temperature been determined for ohmic electrical contacts on any polytype of SiC.

Diodes and more complex devices have recently been fabricated in ß-SiC thin films. Yoshida et al. [39] have produced Schottky barrier diodes on unintentionally doped films grown on Si(100) using Ni and Au as the ohmic and rectifying contacts, respectively. The barrier height, as determined by capacitance and photoresponse measurements, was 1.15 (±0.15) eV and 1.11 (±0.03) eV, respectively. This same group of investigators have also fabricated metal-semiconductor (Schottky-barrier) field-effect transistors (MESFET) by the successive CVD of Al-doped (E17 cm^{-3}), p-type and undoped, n-type ((3-7) E16 cm^{-3}) ß-SiC layers on p-type Si substrates [40]. Gold and Al electrodes were used for the Schottky-barrier gate and the ohmic (Source and drain) contacts, respectively, for the n-type SiC. Gate voltages from -1.0 to 0.6 V were applied. A high channel resistance and a small (10 μA) drain current indicated that the leakage current through both the SiC p-n junction used for isolation of the

device region from the Si substrate and the isolation grooves was not negligible compared with the current through the n channel. A transconductance at saturation of ≃0.09 mS/mm and a threshold voltage of ≃-1.4V were reported. Finally, these researchers have investigated [41] the effect of heating to 573K on the operation of a MESFET similar to that just described but with the Al layer replaced with one containing B and a different configuration of electrodes. At 298K the leakage current was considerably reduced in this sample relative to the Al-doped material; the drain current was almost zero at negative gate voltage > -1.6 V; and a transconductance of 0.5 mS/mm was reported. With increasing temperature, a considerable increase in leakage current was noted and the transconductance was reduced to 0.17 and 0.1 mS/mm in the saturation region at 473K and 573K, respectively. The cause of these changes were postulated to be related in that in the deep depletion mode, the current flow was through the B-doped layers wherein the resistivity was reduced by the increased thermal energy. Conversely, in the enhancement mode, the drain current was reduced by a decrease in the electron mobility with temperature. The drain I-V characteristics were not changed after heating to 573K in air.

In related research, Suzuki and co-workers [42, 43] have fabricated p-n junction diodes having a mesa structure and determined their electrical character to 773K. No significant chemical degradation was observed at any temperature. At room temperature, the device had a forward turn-on voltage of ≃ 1.2V and a reverse leakage current of 5 μA at 5V. However both parameters seriously degraded with an increase in temperature. The curves of forward current density vs. voltage contained three distinct regions at all temperatures which indicated (1) excess currents at applied

voltages lower than ~0.6V, (2) exponentially increasing currents at 0.6-1.1V and (3) gradually increasing currents at voltages > 1.1V.

Finally, Shibahara et al. [44] and Kondo et al. [45] have produced working metal oxide semiconductor transistors (MOSFETs) on ß-SiC films. The MOSFET produced by the former group was fabricated in B-doped, p-type SiC (t~2 μm, p~E15 cm^{-3}) grown on undoped SiC (t~7 μm, n~E17 cm^{-3}) with source and drain formed by ion implantation of P^+ and subsequent annealing at 1353K for 3.6E3s. The leakage current between the source and gate was < 1 μA for the gate bias of ±10 V. By contrast, Kondo and coworkers [45] produced their device on an undoped, n-type SiC layer grown on an Al-doped p-type layer previously deposited on p-type (40-60 ohm-cm) Si substrate. Poly-Si combined with Al metallization was used for the source and drain contacts with SiO_2 as the gate material. Their device also functioned in either the enhancement or the depletion mode. However, considerable leakage current through the p-type layer was evident, as the drain current did not saturate even at drain voltages > -12 V.

The following sections detail the procedures and results of (i) growth of ß-SiC on Si (100) and α-SiC (0001), including theoretical calculations of the compositions and the amounts of condensed product gas phases which are predicted to occur under equilibrium conditions at various Si/(Si+C) ratios, (ii) observation of defect structures in the SiC thin films, (iii) in situ and ion implantation doping of the films, (iv) reactive ion etching, and (v) device fabrication and characterization.

3 EXPERIMENTAL PROCEDURES

Chemical equilibrium calculations involve the computation of the composition of a system, subjected to certain constraints, which contains the minimum free energy. The constraints in CVD systems are the preservation of the masses of each element present, constant temperature, and constant total pressure. White et al. [46] initially developed a computational technique which involves the minimization of the summation of the free energies of all the species present in a given system. Erikson [47] has extended the method to include systems containing more than one condensed phase, including solid solutions, and developed a companion program (SOLGASMIX-PV) for performing the calculations. This program has been used in the present research to calculate the number of moles of the condensed phases which would deposit and to determine the types and amounts of the product gases which would be present under equilibrium conditions. In these calculations, the elements of Si, C and H were the principal species, since SiH_4 and C_2H_4 were the reactant gases, and H_2 was the carrier gas. The total amount of Si and C was maintained at 1 mole; thus, the Si/(Si+C) ratio varied from 0 to 1.0. The substrate was assumed to be inert although, in reality, it has a moderate vapor pressure near its melting point and could, therefore, be a small part of the overall reaction if a high growth temperature is experimentally employed, especially under low-pressure conditions. The thermodynamic values for all species used in these calculations were taken from the JANAF tables [48]. The $H_2/(SiH_4+C_2H_4)$ mole ratio and the total pressure were fixed at 1000 and 1 atm, respectively. The temperature was chosen to be 1630K, which is essentially that used in the growth of ß-SiC on Si substrates.

Epitaxial films of ß-SiC have primarily been grown in this research on chemically converted surfaces of high resistivity (ρ = 5000 - 8000 Ω-cm, p-type monocrystalline Si(100) substrates by CVD using the high-purity gases of silane (SiH_4) (maximum impurity of 5 ppm N_2) and ethylene (C_2H_4) (maximum impurities 25 ppm N_2 and 65 ppm other hydrocarbons) entrained in the purified (Pd/Ag cell) carrier gas of H_2. For the chemical conversion process in our reactor, an experimentally determined optimum amount of 0.30 mole % of C_2H_4 (1 sccm) in flowing H_2 (3000 sccm) is introduced into the cold wall, barrel-type reaction chamber at room temperature. The substrates (and the SiC-coated graphite susceptor on which they rest) are immediately and rapidly heated to 1660K over a total period of 150s to produce a very thin chemically converted layer of monocrystalline ß-SiC [49]. The subsequent CVD growth of ß-SiC(100) films on this layer is achieved by establishing SiH_4 and C_2H_4 flow rates in the 3000-sccm H_2 flow at a temperature of 1660K and 1 atm total pressure. Growth rates are typically 2 μm/h. For a complete review of this process and the results of analyses of the converted layers, the reader is referred to Ref. 49.

The considerable mismatch in the lattice parameters of Si(100) and ß-SiC(100) noted above resulted in the formation of numerous microtwins, intrinsic stacking faults and antiphase boundaries (APB) (see discussion below). As such, investigations concerned with growth on off-axis Si(100) and on the (00001) plane of α-SiC have been conducted. The former approach has been used extinsively by researchers in the GaAs community in their analogous attempt to grow large diameter, monocrystalline APB-free films of this material on Si (100) (for a review of this research, see various chapters in Ref. 50). Moreover, Shibahara et al. [51] have

recently shown that APBs can be successfully eliminated in ß-SiC using off-axis Si(100) with the [100] inclined 2° toward [011]. In our research both 2° and 4° inclinations of the Si[100] toward [011] were investigated; the resultant ß-SiC films were $\simeq$ 5 μm thick after a growth period of 7.2 E3s. Unfortunately, the other types of defects were not eliminated by this procedure.

In an attempt to eliminate all of the various defects simultaneously, growth on the Si (0001) and C (0001) faces of Acheson-derived 6H α-SiC substrates has been studied within the temperature range 1683K-1823K at 1 atm. total pressure and using a SiH_4/C_2H_4 flow ratio of 2. Prior to deposition each 6H SiC was preoxidized at 1473K in a flowing dry oxygen atmosphere for 5.4E3s to remove approximately 50 nm of the as-grown surface. The resulting oxide layer was removed with a 1.1 HF + HNO_3 solution immediately prior to loading on a SiC-coated graphite susceptor. Following evacuation of the growth chamber to 10^{-5} Torr, flowing H_2 (3000 sccm) was admitted into the chamber, the substrates heated at the temperature of growth for 600 s followed by the introduction of SiH_4 and C_2H_4.

The effect of the Si/(Si+C) ratio in the gas stream on the growth rate and the microstructure of the ß-SiC(100) films grown on Si(100) has also been investigated. The variations in this ratio are listed in Table I. For the values of Si/(Si+C) < 0.5, the Si/(Si+C) ratio was varied by keeping the SiH_4 flow rate a constant for each run (2.05_{sccm}) while changing the C_2H_4 flow rate. For Si/(Si+C) > 0.5, the ratio was varied in the reverse way, i.e., by maintaining a constant (1.02_{sccm}) C_2H_4 flow rate while changing the SiH_4 flow rate.

TABLE I. Flow rates of SiH_4 and C_2H_4 used to produce the Si/(Si+C) ratios of this study.

Sample no.	SiH_4 flow rate (sccm)	C_2H_4 flow rate (sccm)	$\frac{Si}{Si + C}$	Thickness (μm)
202	2.04	2.20	0.316	5.0
203	2.04	1.89	0.351	5.6
204	2.03	1.63	0.384	4.9
205	2.08	1.32	0.441	7.4
206	2.09	1.06	0.496	6.7
207	2.15	1.04	0.508	6.9
208	2.30	1.00	0.535	5.4

Device development in our ß-SiC has involved simultaneous investigations concerned with (1) introduction of the n-type dopants of N and P and the p-type of B and Al, (2) dry etching and (3) device fabrication procedures and their employment.

Each of the various dopants noted above were individually incorporated into the films either directly during growth or via ion implantation. In the former procedure, the dopant gases of N (or NH_3), B_2H_6 and Al $(CH_3)_3$ (carried in H_2) were incorporated directly into the primary gas stream. Prior to implantation each sample was mechanically polished, oxidized, and etched in HF in order to obtain a clean, undamaged and smooth surface. The conditions of the implantation experiments are given in Table II. All implants were conducted using an offset angle of 7° from the sample surface in order to ameliorate channeling. As highly damaged or amorphous regions resulted from implantation at both room or LN temperatures, post annealing for 300s at temperatures between 1673 and 32073K was necessary to cause solid phase epitaxial regrowth of the implanted region and the activation of the dopant species. Substantial *in situ* annealing occurred during high temperature implantation; thus a much lower annealing temperature of 1473K (for 1800s) was sufficient to maximize the activation of the dopant series.

The atomic concentrations of the dopants introduced by both methods were measured as a function of depth using secondary ion mass spectrometry (SIMS); corresponding carrier concentrations were determined via differential capacitance -voltage measurements using a H_g-probe. Initial surface related electrical measurements (sheet and spreading resistance) indicated that highly conductive surface layers existed leading to excess leakage current. This phenomenon is explained by the fact that ion bombardment of ß-SiC results in a Si-rich surface layer

TABLE II. Experimental Conditions for the Implantation of Various Ions into ß-SiC Thin Films.

Species	Dose (cm^{-2})	Energy (keV)	Temperature (K)
B	2E15, 1.5E15†	200, 100	LN*
Al	9E114, 6E14†	190, 110	298
	6E14	185	623, 823, 1023
N	1.5E14, 1.1E14†	200, 100	LN*
N	1.3E14, 0.9E14†	180, 90	623
	1.3E14, 0.9E14†	180, 90	823
	1.3E14, 0.9E14†	180, 90	1023
P	1E15	110	LN,* 298
	1E15, 6E14†	220, 110	298

† *Dual implant*

* Sample surrounded by liquid nitrogen; actual sample temperature may be slighlty higher.

as a result of forcing C into the bulk. In subsequent research, this layer was always removed by heating the samples at 1473K for 1800s in dry O_2 and subsequent etching in HF. Structural characterization of the implemented layer was conducted via cross-section TEM and Rutherford Backscattering/channeling; the latter used 2.0 MeV $^4He^+$ ions incident along the <110> axial direction.

Reactive ion etching experiments were performed in a parallel plate reactor (Plasmalab RIE 80) with a 28.0 cm diameter Al anode and a 17.0 cm diameter anodized Al cathode with a plate separation of 5.0 cm. Either the anodized Al cathode or a C coverplate were used to support the samples, which were kept at a temperature of 308K. A 13.56 MHz rf supply powered the cathode at densities of 0.440 to 0.548 W/cm^2. The chamber was evacuated to a pressure of $5x10^{-5}$ Torr and the gas (CF_4 or NF_3) was introduced at 25 sccm, maintaining a pressure of 40 mTorr.

Plasma etching experiments were also performed in a parallel plate system (Plasmalab DP 80) having upper and lower Al electrode diameters of 28.0 cm and 24.0 cm, respectively, and a plate separation of 3.0 cm. the upper plate was powered by a 13.56 MHz rf supply at a density of 0.325 W/cm^2. A base pressure of $5x10^{-5}$ Torr was attained and SF_6 was introduced at 30 sccm, giving a constant pressure of 100mTorr. All etched surfaces were characterized by Auger electron spectroscopy (AES) and scanning elecron microscopy (SEM).

Schottky diodes have been produced on undoped ß-SiC films grown on Si(100) and α-SiC(0001) using small Au rectifying contacts and $TaSi_2$ (on Si) or a large area of Au (on α-SiC) as ohmic contacts. Prior to the fabrication of this and all other devices noted below, particular attention was given to surface preparation, including repeated

acid (H_2SO_4 or HF) and DI washes as well as polishing, oxidation and subsequent etching in HF to remove any contaminants, subsurface mechanical damage and free C.

Both *in situ* doping of Al (7E15 cm^{-3}) and ion implantation of Al (5E14 cm^{-2}, 100 keV at 1023K) or N (1.5E14 cm^{-2}, 200 keV and 1.1E14 cm^{-2}, 100 keV at LN conditions) into n-type (4E16 electrons cm^{-3}) or p-type (4E16 holes cm^{-3}) films, respectively were used to create p-n junctions. Ohmic contacts of evaporated 90/a/o Au/-3a/o Ta-7a/0 Al alloy or pure Al were employed for the Al doped materials; sputter deposited $TaSi_2$ was used for the N implanted sample.

MESFETS were produced in a 60 nm thick, undoped, n-type ß-SiC film epitaxially deposited on a 7 μm thick, buried Al-doped p-type ß-SiC layer previoulsy grown on p-type Si. The latter layer was used to (1) confine the current to a thin n-type active layer and (2) move this active layer away from the defect region which extended ~3 μm from the Si/SiC interface. The carrier concentrations of the n- and p-type layers were 5E16 cm^{-3} and 3E16 - 3E17 cm^{-3}, respectively. The sample was subsequently oxidized in flowing dry oxygen at 1373K for 7.2E3S to grow a 46 nm SiO_2 layer to passivate the as-grown surface. A three level mask set employing a concentric ring geometry wherein the gate pattern completely enclosed the center, 100 μm (drain) contact, was used. The gate length and the source-to-drain distance were 3.5 μm and 10.5 μm, respectively. Sputtered $TaSi_2$ was used as the source and drain ohmic contacts. These contacts were annealed at 1173K for 300 s in vacuum to minimize contact resistance. Thermally evaporated Au was used as the gate rectifying contact.

The aforenoted semiconductor paramter analyzer was used to obtain drain current-drain voltage (I_D-V_D) data.

In the fabrication of MOSFETs, oxidation (in addition to that used to remove subsurface damage and which was subsequently etched away) was performed on p-type ((1.5-3.0)E17 Al/cm^{-3}) ß-SiC (on Si) samples at 1473K for 2.16E3s to produce 50 nm of gate oxide. Poly-Si (530 nm) was then deposited via low pressure CVD at 893K and degenerately doped via P diffusion at 1173K for 300s from a glass layer subsequently removed. A circular gate pattern simillar to that used for the MESFETs was applied via photo resist and the poly-Si stripped from all remaining area. A dual N implant 5E14/cm^{-2} at 70 keV and 3.35E14/cm^{-2} at 40 keV) at 873K produced a dual peak concentration of 5E19/cm^{-3}; the poly-Si acted as an implant mask thus producing a self-aligned gate. The source and drain areas were patterned in dark field and etched with buffered HF for 120 s. Following deposition of 200 nm of $TaSi_2$, the remaining photo resist was stripped and the samples cleaned, heated in (1) vacuum for 300 s to anneal the $TaSi_2$ contacts and (2) forming gas (8% H_2/92% N_2) at 723K for 300 s to anneal the surface states at the oxide/SiC interface.

Depletion mode MOSFETs were fabricated in 1.2 µm thick n-type layers ($n \approx 1{,}3E15$ cm^{-3}) on ≈0.5 µm thick p-type ß-SiC thin films grown by CVD at 1773K on the Si (0001) face of 6H α-SiC crystals. The source of p-type doping ($p = 1.6E216$ cm^{-3}) in the 0.5 µm p-type layer was Al which diffused from the heavily Al doped 6H α-SiC substrate. These acceptor species also highly compensated the n-type layers, thus producing the unusually low carrier concentration. The resulting films were polished, oxidized, etched, cleaned, received a deposition of P-doped

poly-Si and patterned to form the gate contacts similarly to the preparation of the inversion mode devices. Two different gate lengths of 7.2 μm and 2.4 μm were employed. The n^+ source and drain areas were subsequently formed by dual N^+, implants using the same dose and energy parameters employed in the inversion devices. The temperature of the implants was 773K. Windows for source and drain contacts, the TaSiz contacts and their anneal and the annealing of the total device were also conducted similarly to that described ro the inversion devices.

4.1 Deposition Considerations. Thin Film Growth and Defect Formation

Thermodynamic Predictions. The equilibrium number of moles of the two condensed phases of ß-SiC and Si (normalized to a maximum value of 1.0), calculated from the SOLGASMIX-PV program as a function of the Si/(Si+C) ratio, is shown in Fig. 1(A). It is not surprising that the amount of β-SiC has a maximum at Si/(Si+C)=0.5, since the total input amount of Si and C was maintained constant, that is, at 1 mole. No free C or free Si was predicted at ratios less than 0.5. However, in the range of Si/(Si+C)>0.5, free Si was predicted to occur with the ß-SiC in an amount which increased linearly with the increase in the Si/(Si+C) ratio. It should be noted that the calculations also showed that a small amount of free Si should form even at Si/(Si+C)=0.5. Thus, from this viewpoint, the proper ratio for the growth of ß-SiC should be in the carbon-excess region.

Although the product gas phase contains Si, SiH, SiH_4, C_2H_2, C_2H_4, CH_3, and CH_4, the calculations showed that the predominant Si- and C- containing species to be SiH_4 (the same as the reactant gas) and CH_4, respectively. The variations in the total partial pressures of all the Si-containing and all the C-containing product gases as a function of the Si/(Si+C) ratio are shown in Fig. 1(B). Each of the totals of the partial pressures of both the Si- and C- containing gases varied markedly in the Si/(Si+C) range < 0.5 but was constant at 0.5 and at all values of the ratio greater than 0.5. At Si/(Si+C) = 0.5, the total pressure of ail the C- containing gases (it was essentially all CH_4) reached a minimum equilibrium pressure; the total pressure of all the Si- containing gases reached a maximum equilibrium pressure as would be expected, since the amounts of the Si- and C- containing gases are increased and decreased, respectively, from Si/(Si+C) = 0.1.

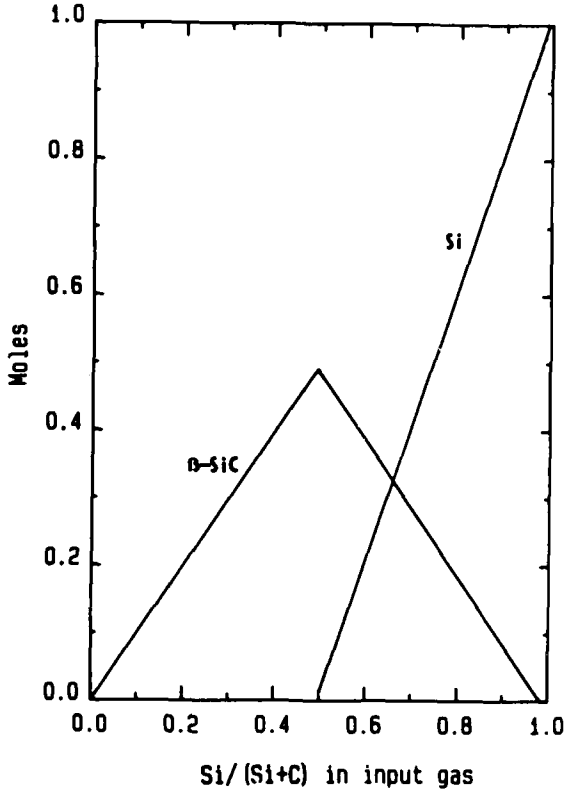

Figure 1A.

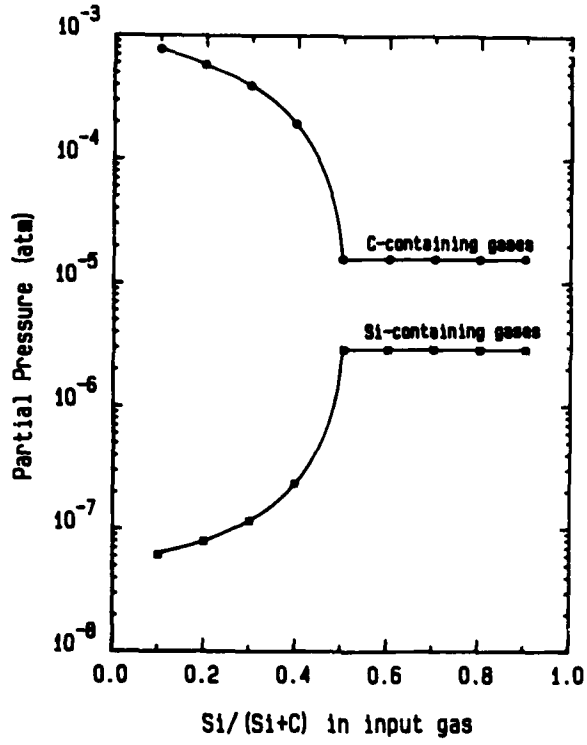

Figure 1B

Figure 1. (A) The amounts of the condensed phases of beta-SiC and Si, as a function of the Si/(Si+C) ratio in the reaction gas stream as predicted from thermodynamic calculations using the "SOLGASMIX-PV" program. (B) The total pressures of all the Si and C-containing gases (expressed as partial pressure of a total gas mixture which also contains H_2) as a function of the Si/(Si+C) ratio in the reaction gas stream. The values noted in the graph were obtained from thermodynamic calculations using the "SOLGASMIX-PV" program.

The constancy in the partial pressure of the C- and Si- containing product gases above Si/(Si+C) = 0.5 occurs primarily as a result of the increasing formation of Si. This combined with the formation of SiC and the decrease in the mole fraction of C_2H_4 entering the gas stream act in concert to maintain the constant partial pressures. At Si/(Si+C) = 1.0, all the SiH_4 is predicted to have reacted to form Si; thus, no Si- or C-containing product gases exist at this point.

As noted above, the results of these thermodynamic calculations indicate that the optimum Si/(Si+C) ratio for the formation of the single phase of ß-SiC under the stated conditions should be slightly less than 0.5. Furthermore, it may be reasoned that the fastest growth rate of the ß-SiC would occur at approximately this ratio as a consequence of the largest amount of this material (although the thermodynamics tells one nothing regarding the kinetics of growth). However, these results must be compared with carefully conducted experiments to determine their approximation to results obtained under the nonequilibrium conditions extant in the CVD reactor.

Effect of Si/(Si+C) Ratio on Deposition Rate and Microstructure. The growth rate of the ß-SC films is shown in Fig. 2 as a function of the Si/(Si+C)=0.496. As the Si/(Si+C) ratio was decreased below 0.5, black inclusions having an average size of 15 µm appeared in the ß-SiC films and increased in size and density as the amount of C in the gas phase increased. Essentially all the inclusions possessed quasi-hexagonal faceting as shown by SEM. SIMS and analytical SEM were employed to chemically analyze the particles. The results derived from both instruments indicated essentially no differences in the concentrations of Si and C in the inclusions and in the ß-SiC matrix. From these results, it may be concluded that the inclusions are SiC particles.

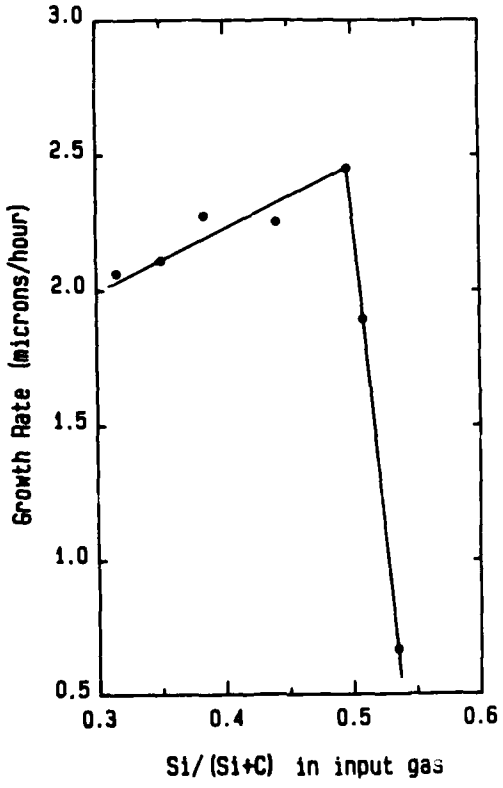

Figure 2. The experimentally determined growth rate of the beta-SiC films as a function of the Si/(Si+C) ratio in the reaction gas stream. The total pressure, H_2 flow rate, temperature, and elapsed time for all depositions was 0.1 MPa, 3000 sccm, 1633K, and 7.2 x 10^3 s, respectively.

Figure 2 also shows that the growth rate is rapidly reduced beyond Si/(Si+C)=0.5. The exact reason for this phenomenon is not known; however, numerous spherical particles occurred in the ß-SiC film growth at Si/(Si+C)=0.535 which were not observed at lower values of this ratio. We believe these particles to be free Si which the thermodynamic calculatons predict should be produced in this range; however, this has not been proven analytically. It is also believed that they are produced by homogeneous nucleation in the gas phase. Moreover, their residence time in the gas phase may allow them to serve as sites for the additional heterogeneous nucleation and growth of Si which would normally have been used in the reaction with C_2H_4 to form SiC. Furthermore, if this process is enhanced by the increase in the amount of SiH_4 in the input gas stream, this could explain the observed rapid drop in the growth rate of the films.

Thin Film Growth and Defect Structures. The ß-SiC layer produced by chemical conversion of the Si (100) surface was monocrystalline and microscopically rough, varying in thickness from 5-12 nm (Fig. 3). It contained a high density of planar defects that were primarily {111} microtwins and intrinsic stacking faults. In addition, localized regions of the converted layer exhibited disorder.

Plan-view and cross-sectional transmission electron micrographs of a ß-SiC thin film are shown in Figs. 4(A) and 4(B), respectively. The micrographs show planar defects on {111} planes that intersect at 90° angles in the <100> projection [Fig. 4(A)] and at 70°32' angles in the <110> projection [Fig. 4(B)]. As in the converted layer, these defects were identified as microtwins and intrinsic stacking faults. The density of defects is higher at the interface; it decreases over a distance of 3-4 µm from the

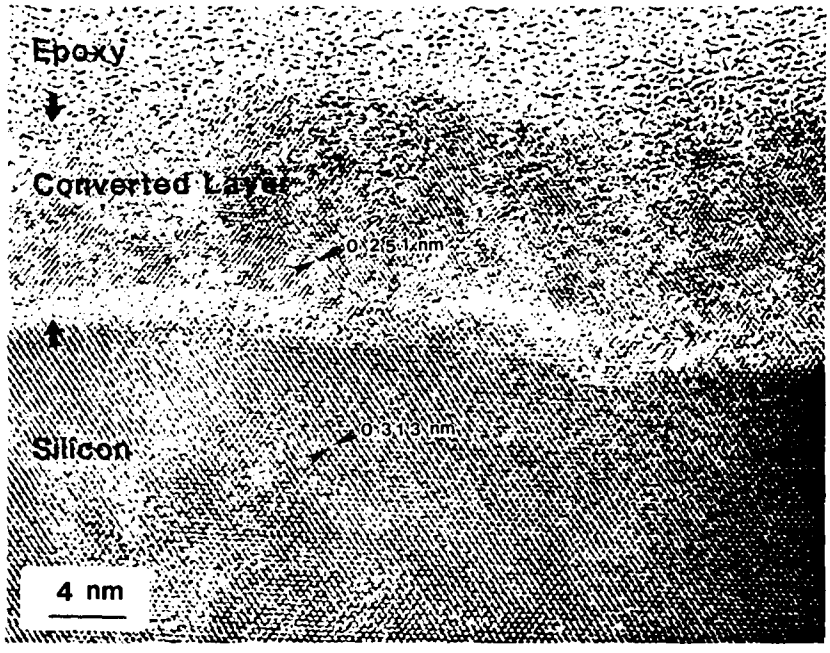

Figure 3. High-resolution XTEM micrograph of converted layer on the Si substrate prior to CVD deposition (courtesy of S. Nutt, Brown University, Providence, RI).

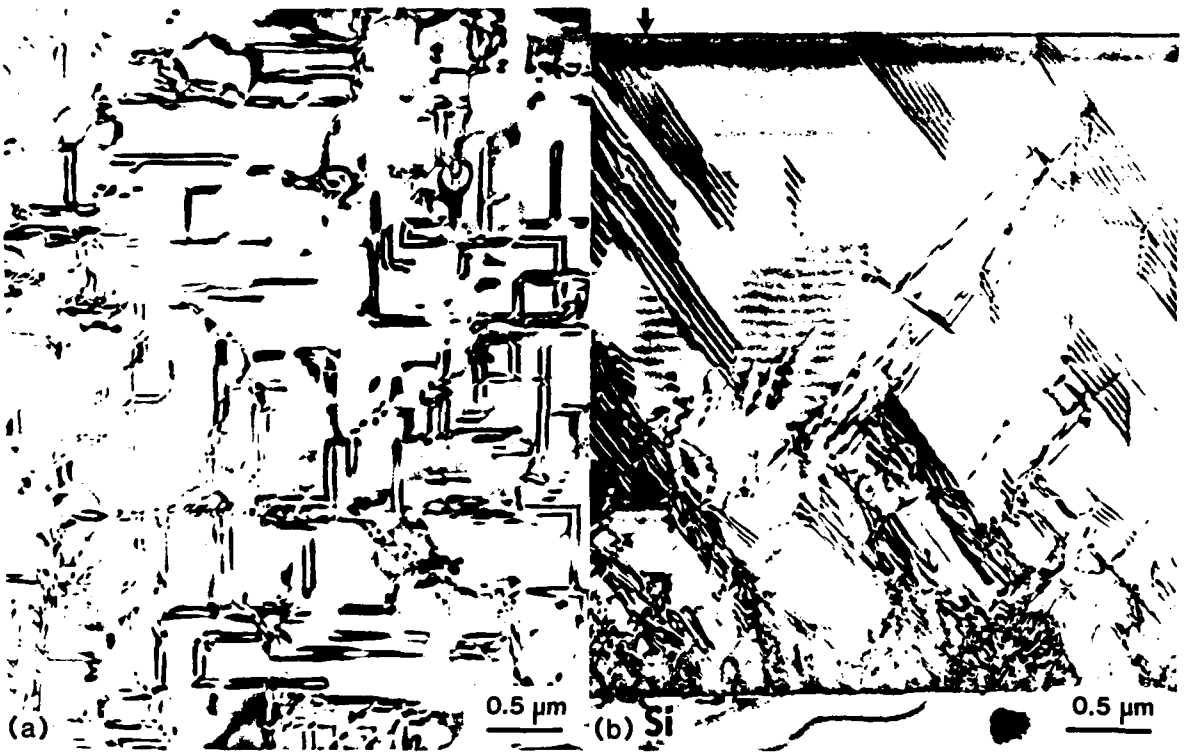

Figure 4. TEM micrographs showing the general microstructure of β-SiC films: (A) ⟨100⟩ plan view showing stacking faults and APBs (arrows); (B) ⟨110⟩ cross-sectional view showing interfacial strain contrast, dislocations, and stacking faults.

interface and becomes approximately constant to the surface even for 20 μm thick films.

There are additional defects in Fig. 4(A) that appear as bands of mottled contrast that extend from the Si-SiC interface to the growth surface (see arrows). These defects have recently been identified as antiphase boundaries (APBs) [52]. The unusual appearance of the APBs may be caused by their interaction with additional defects present in the films. To eliminate these defects, Si substrates with the [100] inclined 2° or 4° toward [011] were used. It has been found that the APBs were eliminated except in the edge regions of the films grown on the 2° off axis Si. A plan-view micrograph of a ß-SiC thin films grown on a 4° off axis Si (100) substrate is shown in Fig. 5. It can be seen that the APBs observed in Fig. 4(A) are no longer present.

The growth of the films on α-SiC substrates has been conducted on both the C (0001) and the Si (0001) faces of the latter material. The resulting film was ß-SiC (111) at all temperatures studied. However, the surface of the film grown on (0001) was very smooth and reflective; whereas, that grown on (0001) was relatively rough and unsuitable for device fabrication. In contrast to films grown on Si substrates, no defects were observed in these films when examined by cross sectional transmission electron microscopy (XTEM) (Fig. 6(A)). In fact, high resolution XTEM shows an abrupt and coherent ß-SiC/α-SiC interfce (Fig. 6(B)). A single atomic layer runs completely across the interface which indicates that the growth direction of the ß-SiC films were exactly [111] in the region (for the growth of ß-SiC on α-SiC C face). However, examination in plan view revealed the presence of double positioning (DP)

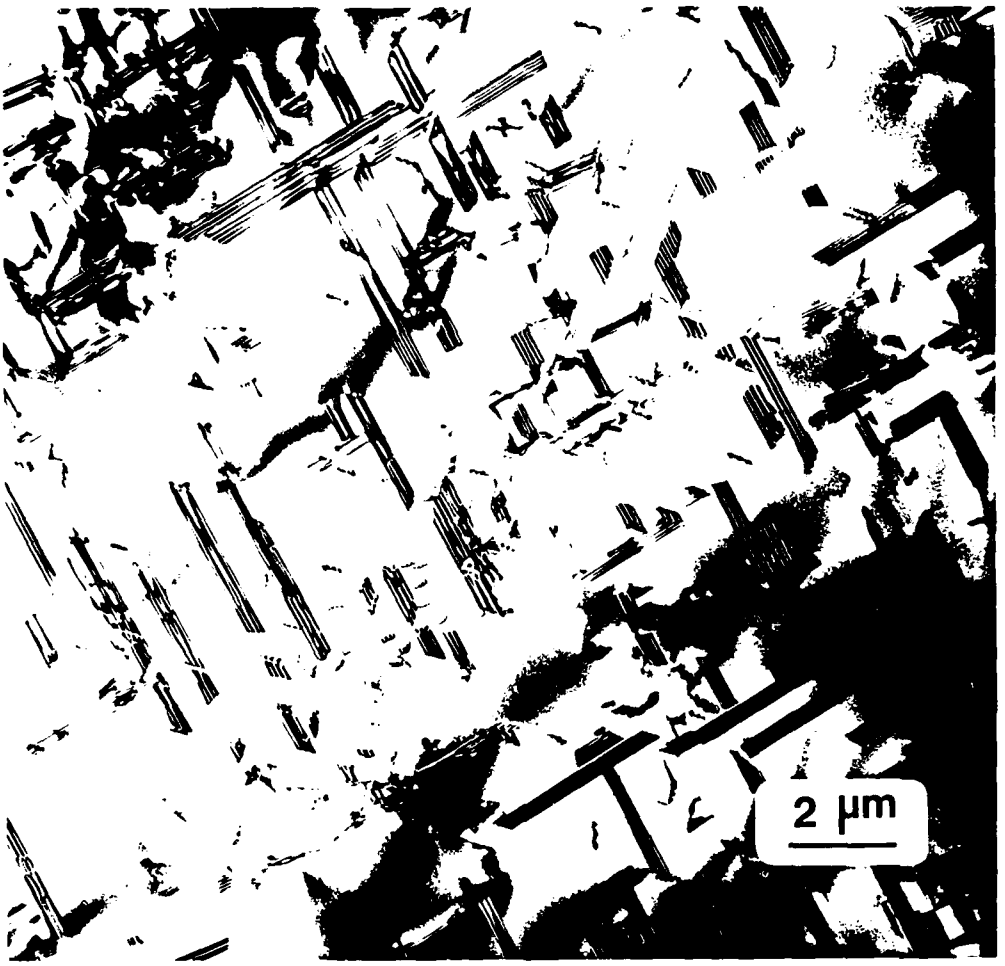

Figure 5. Plan view TEM micrograph showing absence of APBs in the β-SiC film grown on 4° off-axis Si (100), however, stacking faults are still present.

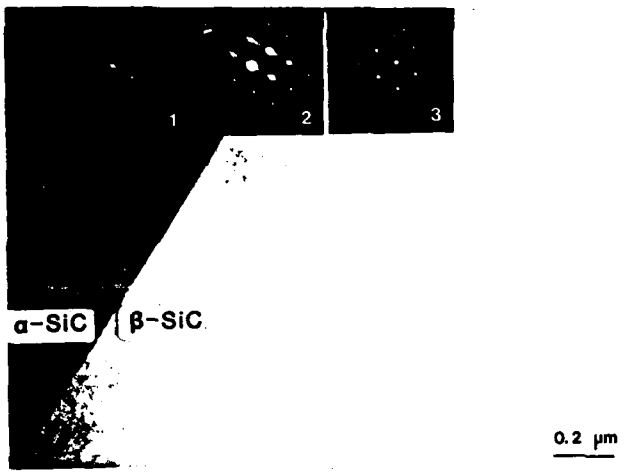

Figure 6(A).

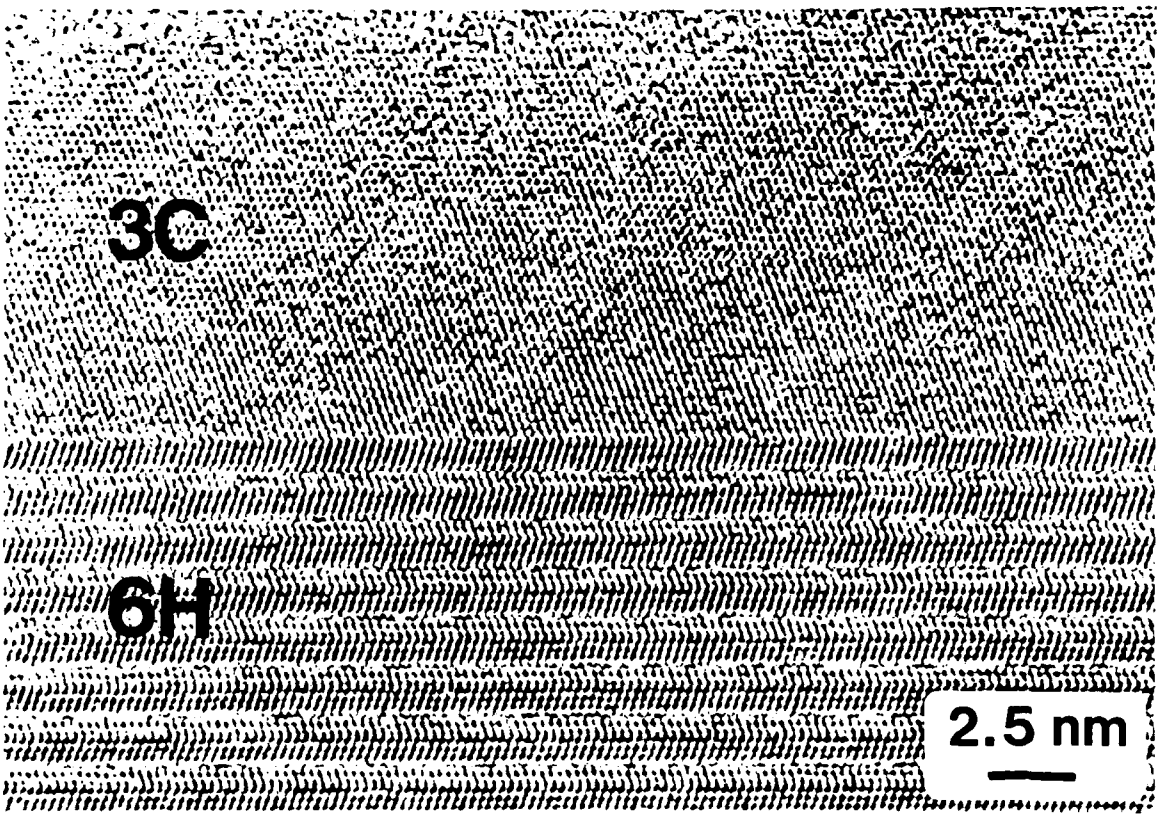

Figure 6(B).

Figure 6. Cross-sectional TEM micrographs of the β-SiC/6H-SiC interface taken at (A) moderate and (B) high resolution (courtesy of Steve Nutt, Brown University, Providence, RI).

boundaries, as shown in Fig. 6(C). In these defects, the material enclosed by the boundaries is oriented 60° to the surrounding matrix and <111>. Very recent research has employed α-SiC crystals with the [0001] inclined 3° toward [1120] heated to 1773K for 600 s. The DP boundaries were eliminated by this procedure and, in contrast to the aforenoted results on this face, for growth the on-axis samples, mirror smooth films were produced. However, the resulting film was the 6H α-SiC polytype. Additional characterization is now ongoing. As a consequence of the very recent nature of this study utilizing α-SiC substrates, the results of most of the remaining research reported below are concerned with ß-SiC grown on Si.

4.2 Impurity Incorporation During Deposition

In-Situ Doping. Figure 7 shows the results of the experimental SIMS measurements of atomic dopant concentration as a function of the partial pressure of the dopant source gas for Al, P, B and N. The linear character of both the curve for Al and the sections of the graphs for P, B and N at lower pressures is predicted from considerations of Henry's law. Moreover these curves are similar to those for dopant incorporation into monocrystalline Si.

Solubility data from direct measurements such as diffusion or lattice parameter studies are not available in the literature for the various dopants for the temperature of 1633K used for the CVD growth. However, the change in slope of the atomic concentration curves for P, B and N as well as the changes in the surface character and the x-ray Laue patterns of these heavily doped samples relative to the undoped (or lightly doped) materials indicate the onset of polycrystallinity. These changes are believed to be triggered by the introduction of the various dopants in excess of their solubility limits. Furthermore, the grain boundaries can act as sinks for excess dopant

Figure 6(C).

Figure 6(C). Cross-sectional TEM micrographs of the β-SiC/6H-SiC interface (C) Plan view of the same film showing double positioning boundaries and associated stacking faults.

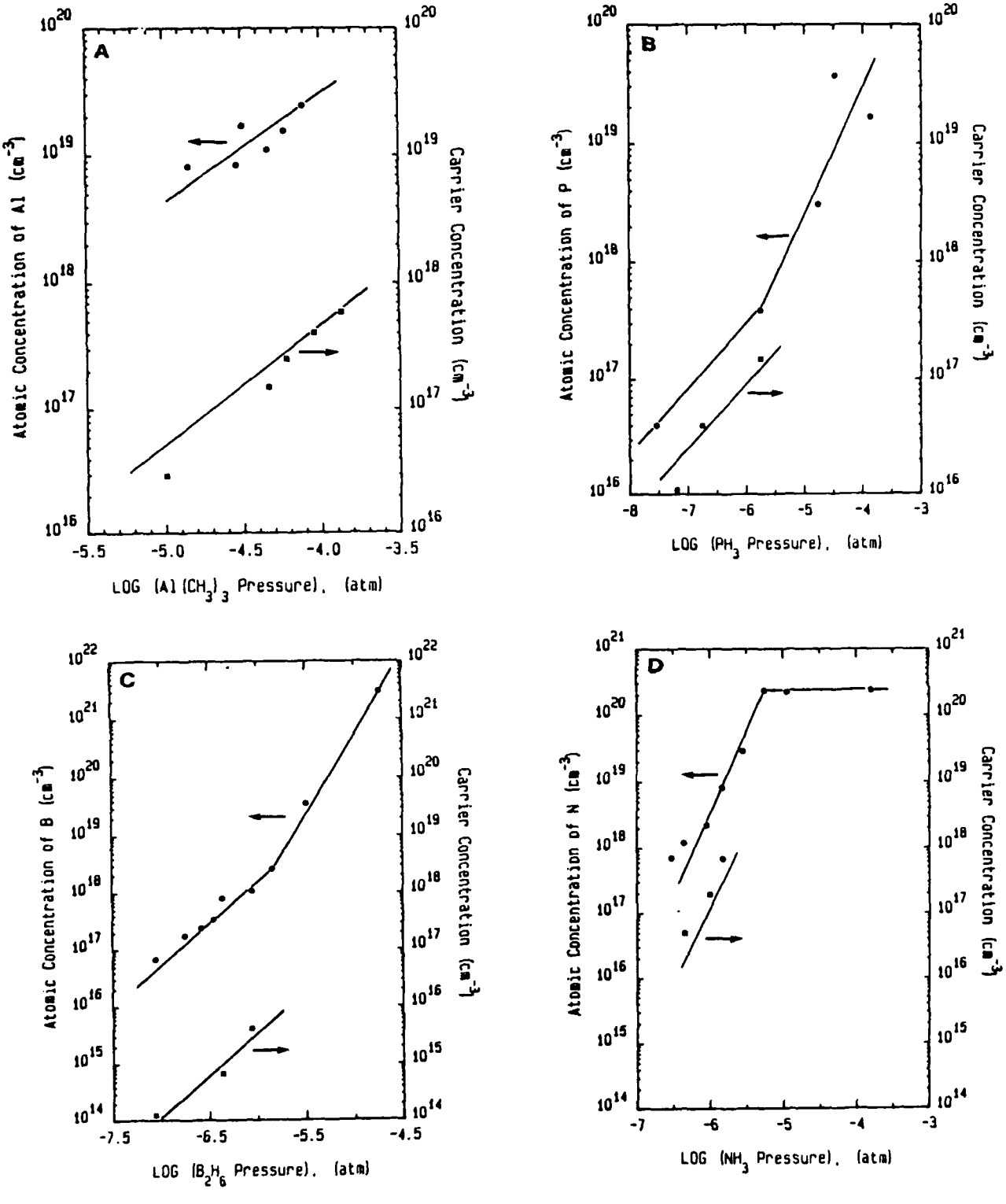

Figure 7. Atomic and carrier concentrations of (A) Al, (B) P, (C) B, and (D) N as a function of the partial pressure in the CVD chamber of the respective dopant gases of $Al(CH_3)_3$, B_2H_6, and NH_3. Aluminum and B are p-type dopants while P and N are n-type dopants in beta-SiC.

and thus allow continued incorporation of these species at levels significantly higher than allowed by the lattice. The maximum in the Al concentration could not be determined because of increased gas phase nucleation and the resultant occurrence of poor films at high TMA input.

The carrier concentrations of each dopant were also found to be a linear function of the partial pressure of the dopant source when plotted on a log-log scale, as shown in Fig. 7. Each figure also reveals a major difference between the atomic concentration and the carrier concentration for each dopant. The reasons for this include the measured deep energy levels for the p-type dopants of Al (0.24 eV) and B (0.735 eV) as well as the possibility of compensation from unintentionally introduced n-type dopants (e.g., N). Other possibilities include (i) compensation from line or point defects and/or trapping of impurities at the dislocations and stacking faults in the material, (ii) dopant-Si and/or dopant-C interaction and (iii) location in nonelectrically active interstitial sites (especially plausible for B). Thus a portion of each of the dopants is either not ionized or located on nonelectrically active sites or complexes with Si or C. Combinations of these events are also probable.

Ion Implantation. Figure 8 (A) shows the buried amorphous layer obtained from a dual B implant using the conditions shown in Table II. This layer extended from 0.1 μm to 0.44 μm beneath the surface. A heavily damaged region extended an additional 0.11 μm into the film. Annealing at 1673K for 300 s caused solid phase epitaxial (SPE) re-growth of the amorphous layer from both crystalline/amorphous interfaces. Two distinct bands of B-containing precipitates, corresponding in position to the two peak maxima of the dual implants also occurred, as shown in Fig. 8(B). No out-diffusion of B was detected as a result of this heat treatment. Annealing at 1873K

Figure 8. Cross-sectional TEM micrographs of β-SiC (100) implanted with B+ at 200 and 100 keV with doses of 2 x 10^{15} cm^{-2}, respectively, at LN temperature: (A) as-implanted; annealed for 300 s at (B) 1673K, (C) 1873K, (Regions a and c contain what are believed to be precipitates, and region b contains what are believed to be both precipitates (small defects) and vacancy loops (large defects).) and (D) 2073K.

(but not lower temperatures) caused the formation of defect clusters, as shown in Fig. 8 (C), at ~ 0.06 μm from the amorphous/crystalline interfaces (regions a and c) and near the center of the original amorphous layer (region b). Those defects in regions a and c have been tentatively identified as precipitates and those in region b as both precipitates and vacancy loops by contrast analysis. Profiling of the B concentration in the 1873K annealed sample via SIMS showed peaks in regions a and c; although diffusion of the B from the original implanted peaks had obviously occurred. Figure 8(d) shows that virtually perfect SPE regrowth, without visible damage, occurred during annealing at 2073K for 300 s. However, SIMS analysis revealed that essentially al the B had diffused away.

The sample from which the micrographs of Fig. 9 were obtained received a dual implant of Al at 298K which produced a buried amorphous layer with a 10 nm crystalline surface, an amorphous depth of 0.17 μm and damage to 0.22 μm [Fig. 9(A)]. Annealing at 1873K for 300 s caused SPE regrowth, but the regrown layer contained many defect clusters [Fig. 9(B)]. A dense band of clusters occurred at a depth from 0.04 to 0.11 μm. When annealed at 2073K (instead of 1873K) for 300 s, the number of defect clusters was after the 1873K anneal did not remain after the 2073K anneal. Some microfaulting was observed in the regrown layer where precipitation was greatest. [See areas labeled X in Fig. 9 (C).] In this case, SIMS showed a decrease in the concentration of Al by a factor of two-to-four throughout most of the profile depth; however, it was slightly increased at the sample surface.

The implantation of N under liquid nitrogen (LN) conditions within the ranges of dose and energy shown in Table I produced a heavily damaged but crystalline layer, as shown by the representative micrographs of Fig. 10. Annealing of the sample

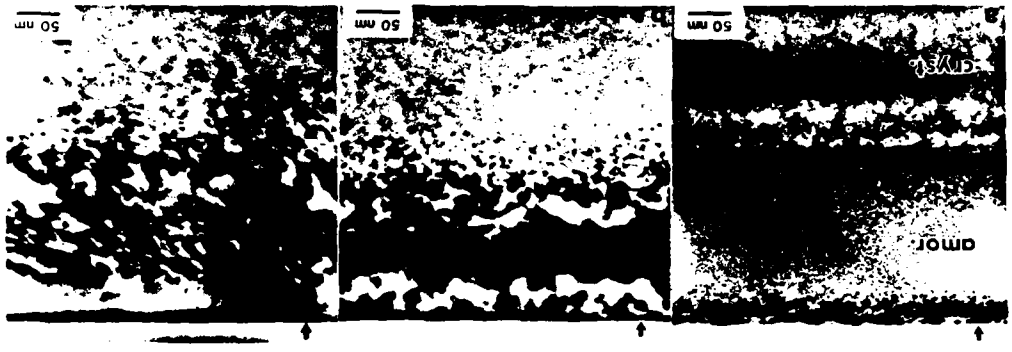

Figure 9. Cross-sectional TEM micrographs of β-SiC (100) implanted with Al+ at 190 and 110 keV with doses of 9 x 10^{14} and 6 x 10^{14} cm^{-2}, respectively, at 298K: (A) as-implanted, (B) annealed at 1873K for 300 s. The upper and lower bands of defects correspond to the original amorphous crystalline interfaces. The band of defects in the center corresponds to the projected range of the implant, (C) annealed at 2073K for 300 s. Note that there are fewer defects than in (B), and the upper band of defects did not form.

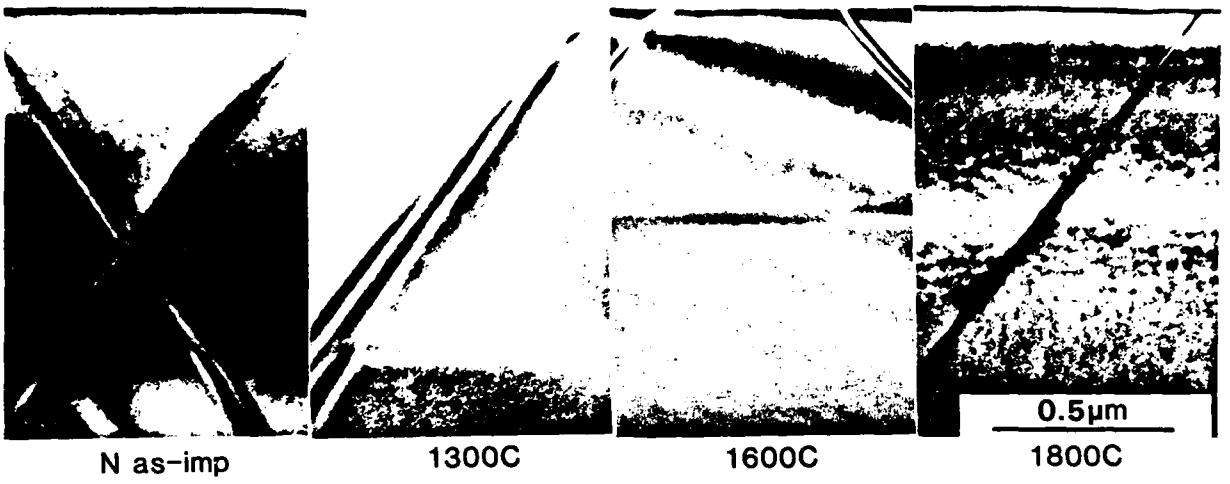

Figure 10. Cross-sectional TEM micrographs of β-SiC (100) implanted with N+ at 200 keV and 100 keV with doses of 1.5×10^{14} cm^{-2}, respectively, at; N temperature (A) as implanted; annealed at (B) 1573K, (C) 1873 and (D) 2073K. A heavily damaged layer was produced but not amorphized during implantation; annealing at 1873K and 2073K resulted in substantial loss of N to the surrounding atmosphere.

above 1573K caused structural rearrangement. No visible damage was observed. Annealing at 1873K or 2073K for 300 s caused considerable out diffusion of N which resulted in a high concentration of this species in the near-surface region.

The effect of implantation at room temperature vs LN conditions on the extent of amorphization is illustrated in Fig. 11. Both micrographs are of films that were implanted with P using the same dose and energy but the sample in Fig. 11 (A) was implanted at 298K, while the sample in Fig. 11 (B) was maintained under LN conditions. The 298K sample had a 10 nm crystalline surface, an amorphous depth of 0.13 μm, and visible damage to 0.23 μm. The LN implant created a thinner crystalline cap (~ 5 nm), an amorphous depth of 0.17 μm, and visible damage to 0.35 μm. The same effect of similar magnitude has been observed in Si wafers implanted at 298K and LN [53]. This similarity was unexpected, as the melting temperature of SiC is > 3073K, while that of Si is 1679K. Annealing studies at 1973K for 300 s using samples containing a dual implant of P (220 keV, 1E15 and 110 keV, 6E14) revealed that the buried amorphous layer became saturated in P causing the layer to regrow in a polycrystalline microstructure after the first 100 nm. Even in this latter region many small precipitates and loops were observed.

As shown by the TEM results, little success was achieved in affecting precipitate- and/or damage-free SPE regrowth in ß-SiC films previously amorphized by ion implantation. In addition, no pronounced changes in the electrical properties of any of these films occurred until anneal temperatures equal to or in excess of 1673K were employed. As such, high temperature implantation is currently being studied to surmount some of these problems. To date, we have learned that implantation of Al or N at 623K, 823K, and especially 1023K (see Table I), allows sufficient *in situ*

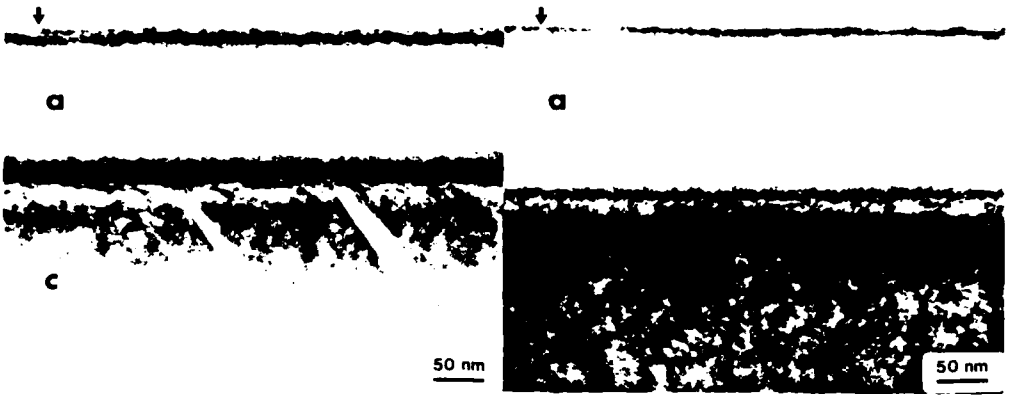

Figure 11. Cross-sectional TEM micrographs of β-SiC (100) implanted with P+ (110 keV, 1 x 10^{15} cm^{-2}): (A) implanted at 298K, (B) implanted at LN temperature. The LN implant has a significantly thicker amorphous region.

annealing during implantation to produce both essentially damage-free implant regions as well as virtually complete electrical activation of the implanted species. The backscattering spectra from the 1023K implants nearly coincide with the aligned spectrum of the unimplanted material. In addition cross-sectional TEM analysis revealed that implantation at this highest temperature resulted in neither visible lattice damage nor precipitates obtained from the anneals of the low temperature implants. Figure 12 shows a comparison of the implanted regions produced at 1023K and under LN conditions. Finally, it should be noted again that a slight increase in the electrical activation of the high temperature implants can be achieved if the samples are annealed at 1473K for 1800 s; however, this is far below the temperatures needed for this process in the samples implanted under 298K or LN conditions.

4.3 Dry Etching

For reactive ion etching of ß-SiC, the choice of cathode material played a major role in the chemical and physical characteristics of the etched surface. Anodized Al cathodes were found to cause micromasking of the SiC during etching, as evidenced by the detection of this element on the etched surfaces. (Fig. 13) and the presence of surface roughness. The degree of roughness also depended on the choice of fluorinated gas, with the faster etching NF_3 causing more roughness (See Fig. 14) than CF_4 employed under the same conditions. The use of the Al cathode also caused accumulation of F in both gases used, allowing it to polymerize with the C on the SiC surface (Fig. 13). The use of a C cathode coverplate ameliorated the micromasking problem and left a smooth and chemically clean surface, with little or no fluorocarbon polymerization, as shown in Fig. 15. This decrease in roughness was especially true with the C cathode/NF_3 combination, as revealed in Fig. 16. Plasma

Figure 12(A)

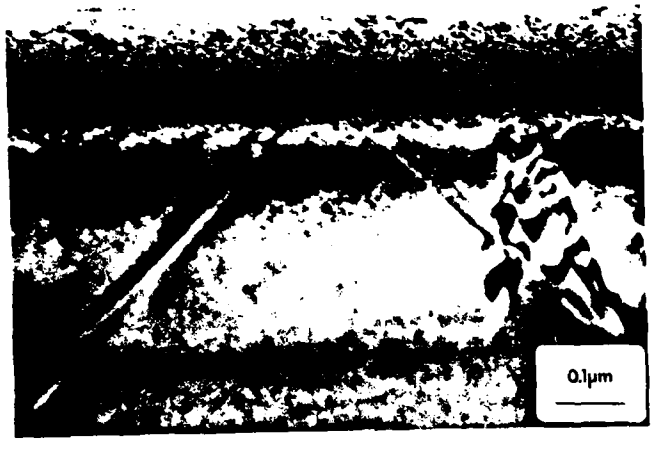

Figure 12(B)

Figure 12. Cross-sectional TEM micrographs comparing the near-surface damage created by implantation of Al to a peak concentration of 4×10^{19} Al/cm^3 at (A) 1023K and (B) LN temperature.

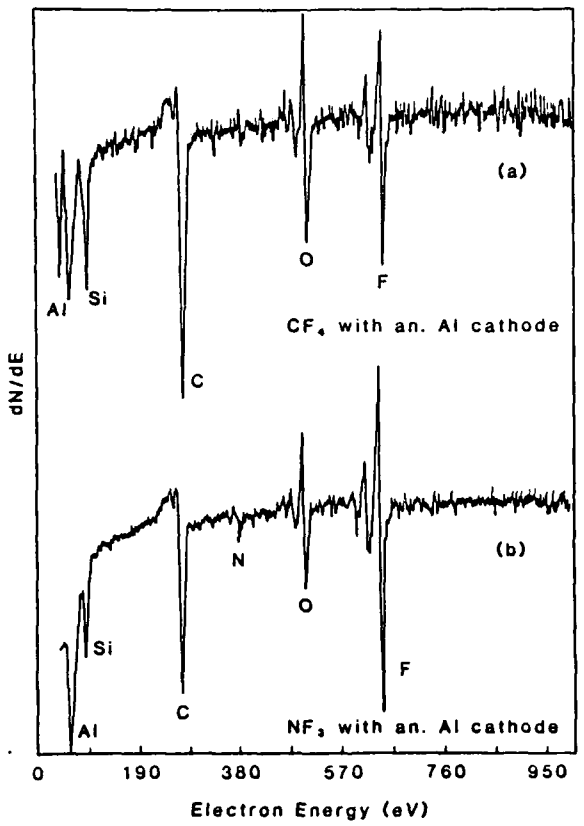

Figure 13. Auger spectra obtained at 2 kV and 0.5 μm for SiC after RIE in (CF_4 on an anodized Al cathode, and (B) NF_3 on an anodized Al cathode, at 40 mT and 0.440 W/cm^2 for 10 min.

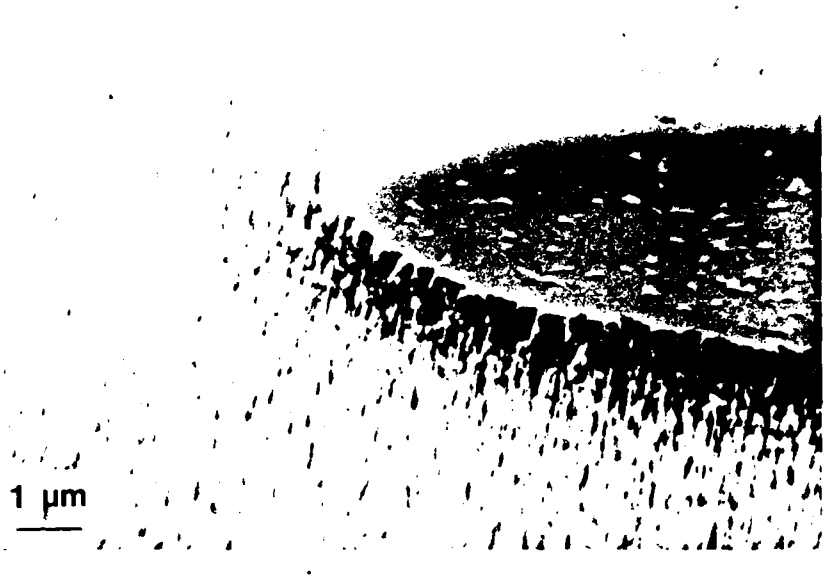

Figure 14. Roughened etched surface of SiC after RIE in NF_3(40 mT, 0.440 W/cm^2) on an anodized Al cathode.

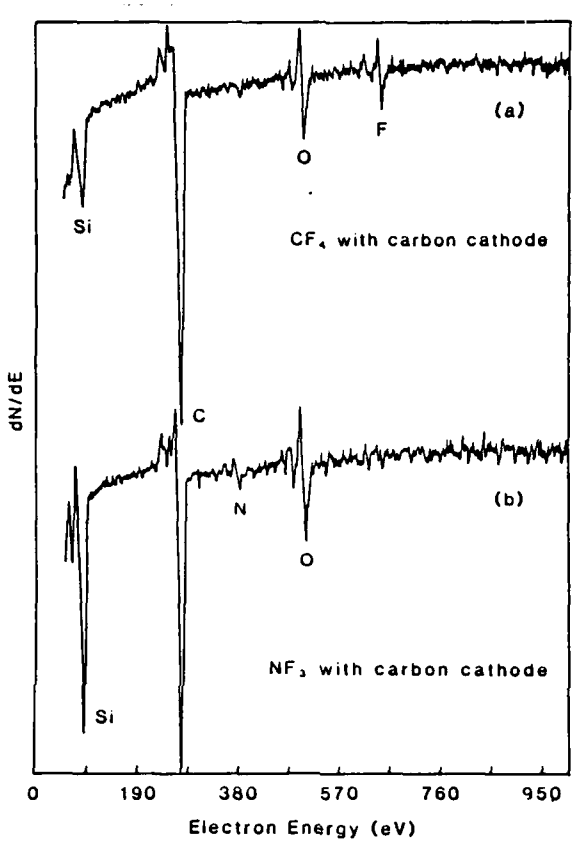

Figure 15. Auger spectra obtained at 2 kV and 0.5 μA for SiC after RIE in (A) CF_4 on a carbon cathode, and (B) NF_3 on a carbon cathode, at 50 mT and 0.440 W/cm^2 for 10 min.

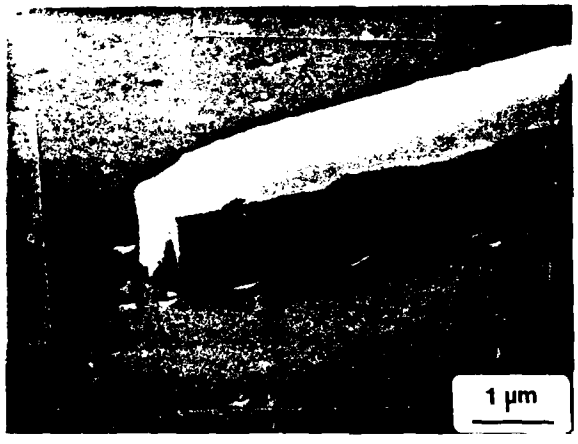

Figure 16. Smooth etched surface of SiC after RIE in NF_3 (40 mT, 0.440 W/cm^2) on a carbon cathode.

etching in SF_6 caused crystallographically spiked formations but left a very clean surface that actually had less native oxide than unetched ß-SiC.

4.4 Device Fabrication and Characterization

Schottky Diodes. The I-V curves for the Schottky diodes produced on the undoped ß-SiC film grown on Si (100) showed significant leakage current (e.g., 0.558 mA at -50 V); however, actual breakdown did not occur up to -100 V. The diode ideality constant from the straight line portion of the curves of log I vs. forward bias V was 2.5; the saturation current was $1\text{-}9 \times 10^{-9}$ A/cm^2, and the barrier height of the Au/ß-SiC junction was calculated to be 0.9 eV. A more accurate value of 1.1 V for this last parameter was obtained from C-V data. Similar measurements and calculations for diodes produced on films grown on α-SiC(0001) gave an ideality factor of 1.6, a saturation current of 1.4×10^{-11} A/cm^2 and a barrier height (from log I vs. forward bias V) of 1.03 eV. The various values of barrier height are close to the previously reported values of 1.11 and 1.15 eV [39] noted above.

Generally in covalent semiconductors like SiC, it is well known that the Fermi level is pinned by the surface states so that the barrier height hardly depends on the work function of the metals and is about two-thirds of the band gap (Eg) of the semiconductor [54]. However, as the band gap of beta-SiC at room temperature is 2.3 eV, the measured values of the barrier height in this research are approximately one-half of the band gap energy. This ratio of $\simeq$ 1/2 was also reported by Hagen [55] as a result of an extensive study of metal/6H-SiC junctions. The barrier height was also independent of the work function of the metal used (Au, Ag and Al). Wu and Campbell [56] also obtained similar values of the barrier height in the Au/6H-SiC system. Thus it appears that the values of the barrier height in metal/SiC contacts

corresponds to one-half, rather than two/thirds, of the band gap energy for both 6H- and beta-SiC.

P-n Junctions. The p-n junction mesa diodes produced by in situ doping showed abrupt interfaces both in SIMS depth profiling and spreading resistance measurements; however, more extensive electrical studies have been conducted only on the junctions produced via implantation. The characteristics of the first diode *in situ* doped with Al and dual implanted with N^+ at LN temperature were rather poor. Typical values of the ideality factor and saturation current were 3.4 and $9x10^{-10}$ A/cm^2, respectively. The leakage current of this diode was negligible up to -5 volts. Abnormal $1/C^2$-V relationships in this diode were the first indication of the insulator nature of the junction. This latter phenomenon has been extensively studied in the Al implanted material, as described below.

Linear I-V plots for either the N or the Al implanted materials were typical of a p-n junction. However, the similarity to a true diode ended at this point. The log I vs. log V character of these diodes is analogous to that observed for current injection into an insulator or wide bandgap semiconductor. For the purpose of illustration of the phenomenon in such materials, consider the four log I vs. log V graphs in Fig. 17. Fig. 17 (A) represents an ideal insulator where I V^2, indicating space-change limited curent flow. In other words, there are no thermal free carriers resulting from impurity-band or band-to-band transitions; the conduction is only within the conduction band as a result of injected carriers. Figure 17 (B) is representative a trap-free insulator in which the current is dominated by the number dominated by the number of thermal free carriers, (n_{ij}) above this point. If shallow electron traps are present, the I-V curve will be shifted, toward higher voltages as a result of trapping. This is shown in

Fig. 17 (c) where the I V and I V^2 sections of the plot again represent currents resulting from thermal free and injected carriers, respectively, but which have been decreased in value by the number of carriers trapped. The vertical portion of the curve occurs when all the traps are filled. An I V^2 relationship again pertains at higher voltages where one achieves pure space-charge limited conduction.

Finally, Fig. 17 (D) illustrates the case of a material with deep traps which have become by thermal free carriers at or below the voltage where injected carriers dominate current flow. A transition subsequently occurs to the point where space-change limited conduction occurs.

A comparison of these representative curves with those derived from our I-V measurements for an Al implanted p-n junction (Figs. 18 (A,B)) log current density (A/cm^2) vs. log forward voltage (V)) shows that room temperature, I $V^{1.8}$ at low and high voltages. Moreover, these two segments are separated only by a transition region which indicates that it contains shallow traps, probably derived from the ionized Al centers. By contrast, an increase in temperature to 473K results in I V at low voltages which is followed immediately by a transition to a segment where I $V^{1.8}$. This is indicative of the effect of deep traps which are believed to be the same source which causes the considerable compensation in the unintentionally doped material [60].

A similar comparison for N implanted into an Al-containing material with the representative curves reveals the reverse of the characteristics for the previous material, i.e., the presence of deep level traps at room temperature and shallow traps at 573K.

MESFETs. Typical room temperature drain current vs drain voltage (I_D-V_D)

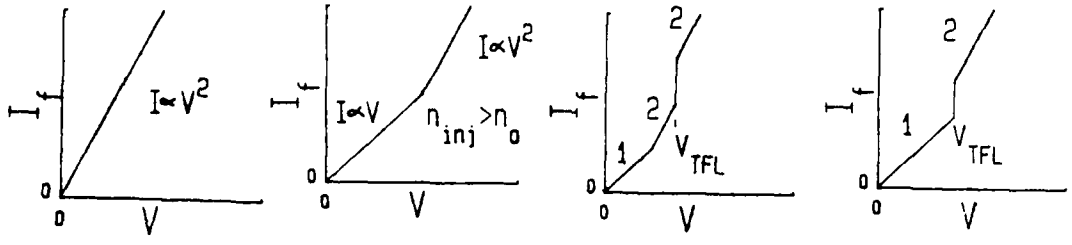

Figure 17. Representative log 1 vs. log V curves for (A) an ideal insulator (space-charge limited current), (B) a trap-free insulator with thermal free carriers, (C) an insulator with shallow traps and thermal free carriers and (D) an insulator with deep traps and thermal free carriers.

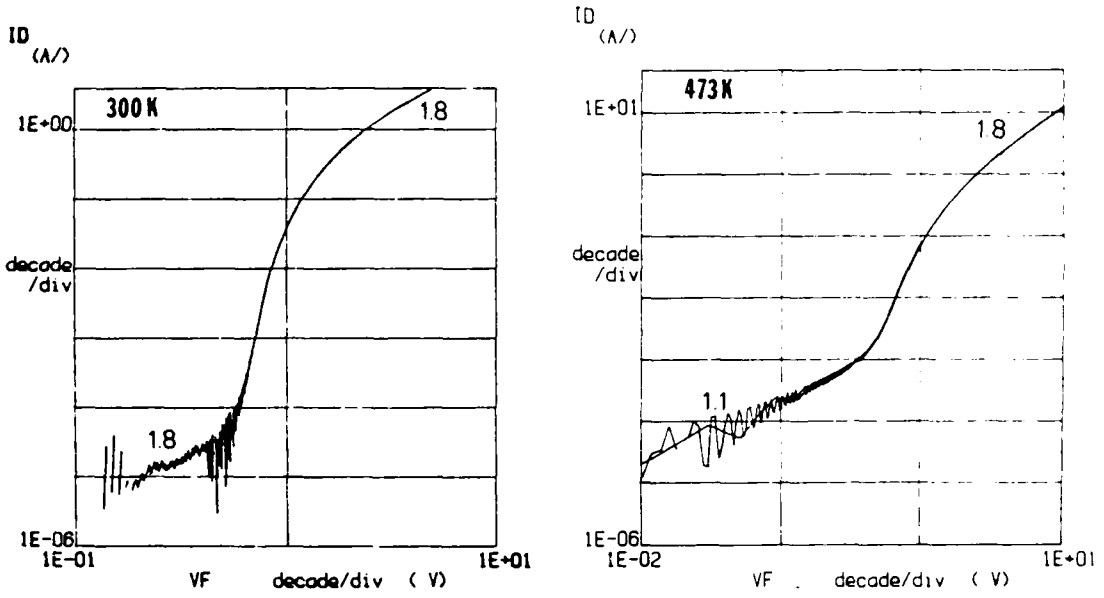

Figure 18. Log I_D vs. log V_F plots for an Al-implanted β-SiC mesa diode where (A) shallow trapping and (B) deep trapping was observed.

characteristics of the MESFETs are shown in Fig. 19. The gate voltage (V_G) was varied from 0.6 V to -1.5V in -0.3V steps. It can be seen that very good drain current saturation is achieved as the drain voltage increases. The maximum transconductance in the saturated region for this device was 0.64 mS/mm, however, a maximum transconductance of 1.6 mS/mm was measured on other devices in this sample. The threshold voltage was -1.6 V, although after subtracting the leakage current, it is reduced to -1.4 V. It was observed that for $V_G < -2$ V the drain current was almost independent of the gate voltage, and thus the device could not be fully turned off. For example, for the device in Fig. 19, the drain current was 2 μA at a drain voltage of 4 V and a gate voltage < -2.5 V. This indicates that there is some leakage current between the gate and drain. This leakage may be caused by the p-n junction underneath the thin n layer, by the leakge current between the gate and source and/or by the defects in the ß-SiC film. As previously reported, [58, 59] the defect density, including the antiphase domain boundaries in the bulk of the film, is very high. Research is underway to fabricate MESFETs in films grown on α-SiC, since it has been shown that these films do not appear to contain any antiphase domain boundaries and much fewer line and planar defects than films grown on Si (100) substrates [60]. This will allow the determination of the role of these defects with regard to leakage current in the film.

MESFETs were also examined at temperatures as high as 623K; a limit imposed by the maximum temperature of the experimental arrangement rather than the devices. Figure 20 shows examples of these measurements on the same device used to determine the room temperature data of Fig. 19. In these measurements the drain voltage was applied from 0 to 10 volts in order to more clearly illustrate the

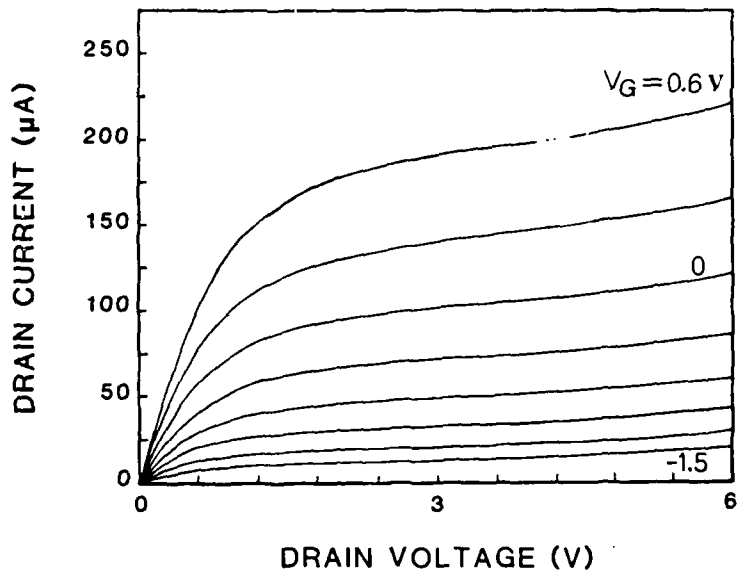

Figure 19. Drain current-voltage characteristics at room temperature of a MESFET with a gate length of 3.5 μm at room temperature and fabricated in a β-SiC (100) monocrystalline film deposited on a Si (100) substrate.

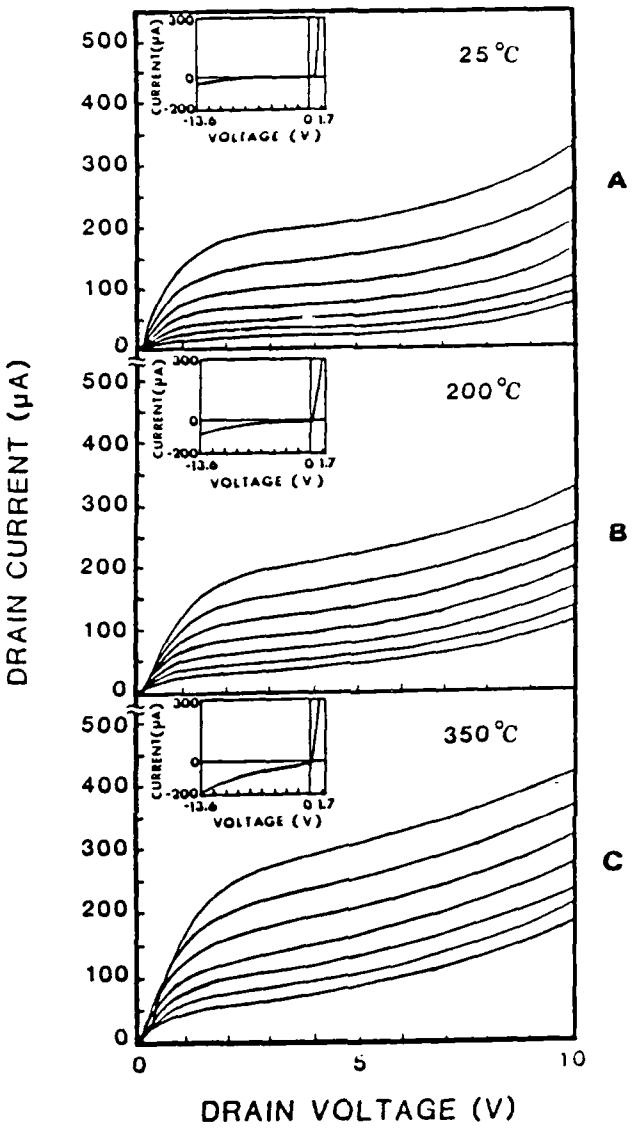

Figure 20. Drain current-voltage characteristics of the MESFET used to obtain the data in Figure 19. (A) Room temperature, (B) 473K and (C) 623K. The current-voltage characteristics of the gate-drain Schottky diode are included as insets at each temperature.

dependence of the I_D - V_D characteristics on temperature. Inset in these figures are the I-V characteristics of the gate-drain diode at the various temperatures. It can be seen that as the temperature was increased, the MESFET drain current achieved less saturation and the gate-drain diode (see inset) at reverse bias yielded more leakage current. At room temperature, this diode leakage current was 5 μA at 8.5 V reverse bias, whereas, at 623K it increased to approximately 70 μA. This was probably caused by an increase in the generation current in the depletion region as temperature was increased. These generated carriers also contributed to the drain-to-source leakage current. The maximum transconductance of this device decreased approximately 21%, as the temperature was increased to 623K. This was expected because electron mobility decreases as temperature increases due to enhanced lattice scattering.

MOSFETs. Figure 21 (A) shows the room temperature I_D vs V_D characteristics for an inversion MOSFET having a 20 μm gate length over the gate voltage range of -4.0 to +8.0 V. The leakge currents at V_D = 5 V and 10 V were < 10 μA and were -2.4 volts and 0.335 mS/mm respectively. This device also showed good stability as a function of temperature to the highest measure point of 673K, as shown in Fig. 21 (B). However, the leakage current increased steadily with temperature to a maximum of 85 μA at 5 V and 673K. The transconductance and threshold voltge range increased to 0.421 mS/mm and decreased t -5 to -6 V, respectively. This negative shift in threshold voltage with temperature was caused by a change in the barrier height between the metal and the semiconductor.

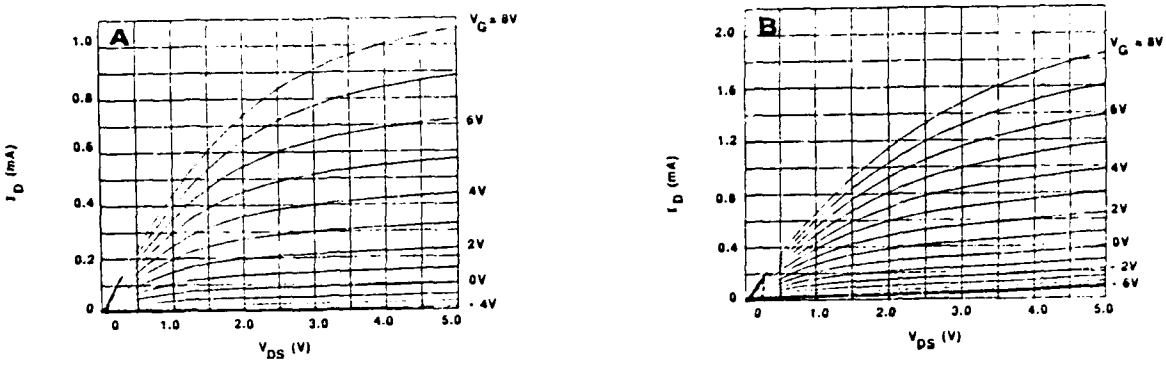

Figure 21. Current-voltage characteristics of a β-SiC n-channel MOSFET with a channel width and channel length of 421 μm, respectively, at (A) 300K and (B) 673K.

Decreasing the gate length to 3.5 μm also produced a stable device at 673K; however, the leakage current was markedly higher (760 μA at V_D = 5 V) than for the 20 μm device at this temperature and dominated the current at high drain voltages. The maximum transconductance at (V_D = 3.0 V) again increased from 0.58 mS/mm at room temperature to 1.65 mS/mm at 673K.. The threshold voltage decreased from 0 V to -2.5 V over the temperature range.

The drain current-voltage characteristics of depletion MOSFET in ß-SiC (111) at 296K are shown in Fig. 22 (A). This particular device had a gate length and width of 7.2 μm and 390 μm, respectively. The source contact to drain contact distance was 24 μm. The device showed very stable drain current saturation out to a drain-source voltage of 25 V. (This trend actually continued to $V_{DS} \approx 30$ V, at which point the oxides underwent breakdown.) The threshold voltage was determined to be at a gate voltage, V_G, of -12.9 V from a plot of $\sqrt{I_{DS(sat)}}$ versus V_G. The leakage current at V_{DS}=25 V in the "off" state (V_G=-15 V) in this device was 3.75 μA. The negative threshold voltage was due, in part, to the voltage required to deplete the n-channel, but it was made more negative by the presence of either fixed oxide charge or mobile ion charge in the range of 5-6x10^{12} cm^{-2}, as obtained from MOS C-V curves of the gate oxide. The 723K anneal in forming gas did not change the threshold voltage. The maximum transconductance of this device at room temperature with V_{DS} fixed at 20 V was 5.32 mS/mm at V_G = 2.5 V.

When this device was heated to 573K and allowed to stabilize for 15 mins., the transconductance actually increased to a maximum of 6.00 mS/mm at V_G=5.5 V and

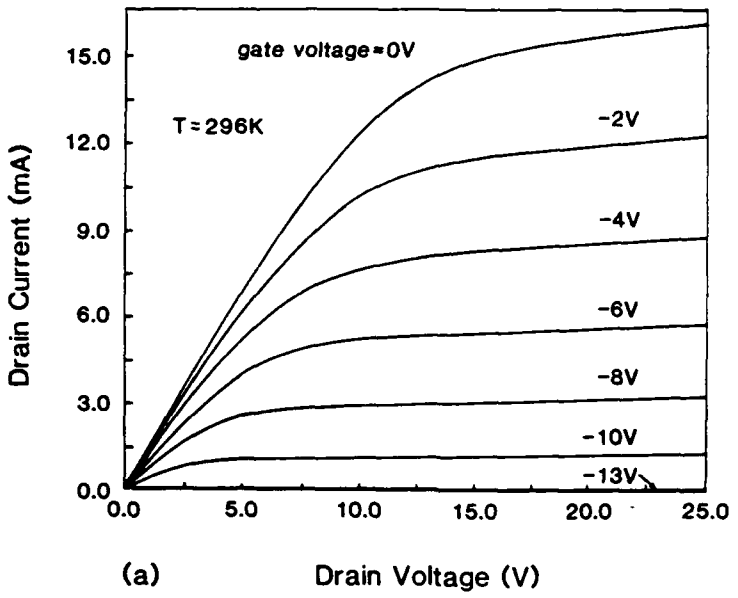

Figure 22(A). Drain characteristics of depletion mode n-channel MOSFET in β-SiC (111) thin film at 296K. The gate length and width of this device was 7.2 μm and 390 μm, respectively.

V_{DS}=20 V. This trend can also be observed by the increased current at V_G=0 V in the 573K drain characterisitcs shown in Fig. 22 (B). The reason for this increase is currently under investigation. Despite the increase in temperature, the drain current saturation was still very stable to V_{DS}=25 V. The leakage current at V_{DS}=25 V and V_G=-15 V increased to 22μA, and the threshold voltage shifted negatively to V_G=13.3V.

The drain characterisitcs of this depletion device were also determined at 673K and at every 50K interval to a maximum of 923K. Results for this last temperature are shown in Fig. 22 (C). The transconductance remained unchanged at 673K; however, it decreased with futher increases in temperature. The maximum transconductance measured was 11.9 mS/mm in a 2.4 μm gate length device at 673K. The lower transconductance of the device in Fig. 22 (C) at 923K is demonstrated by the lower current at V_G=0 V, as compared with the previous curves. Although the transconductance at this temperature became very erratic above V_G=1 V, it reached a maximum of about 4.8 mS/mm of about 4.8 MS/mm at V_G=8V and V_{DS}=20V. The decrease in transconductance above 673K is due to increasing lattice scattering with temperature. The threshold voltage again shifted negatively, to V_G=-14.8 V at 923K. The leakage current increased to 128 μA at V_G=-15 V and V_{DS}=25 V. When the temperature was raised to 973K, this device showed similar current saturation, but the gate oxide experienced breakdown. Thus, current was being injected at the gate and the device could not be cut off.

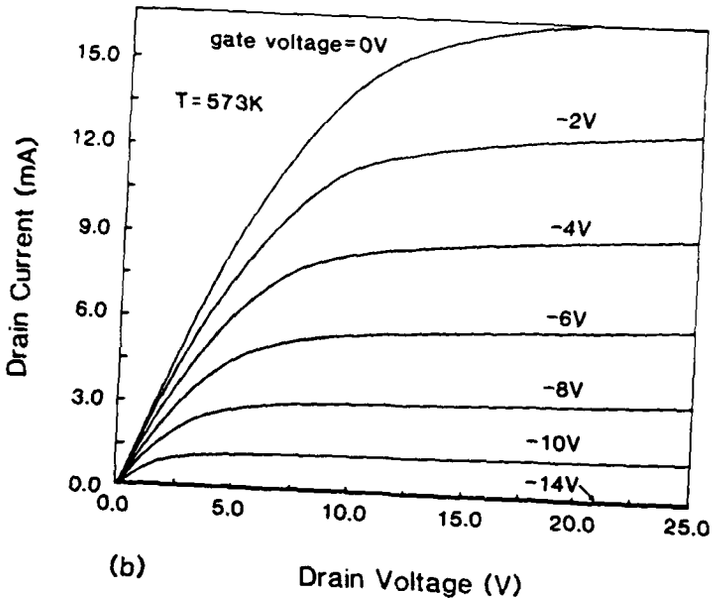

Figure 22(B)

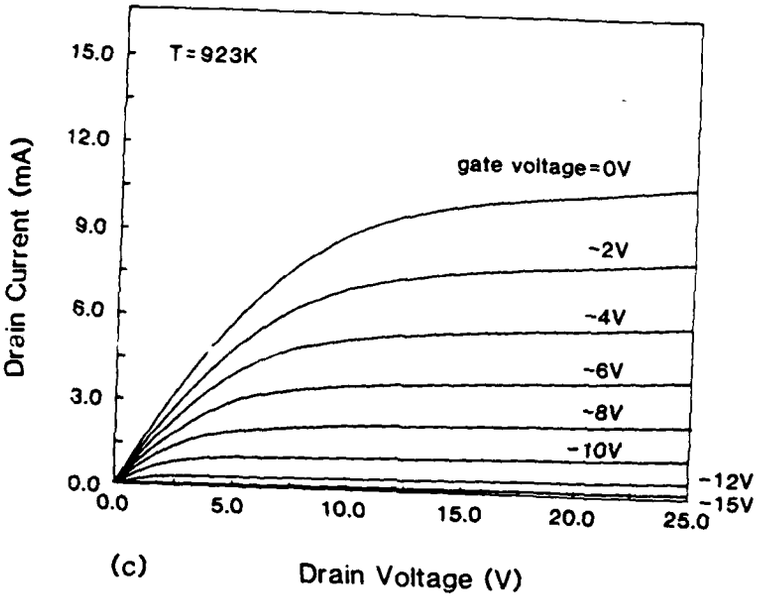

Figure 22(C)

Figure 22. Drain characteristics of depletion mode n-channel MOSFET in β-SiC (111) thin film at (B) 573K and (C) 923K. The gate length and width of this device was 7.2 μm, respectively.

CONCLUSIONS

Monocrystalline thin films of high purity ß-SiC have been grown directly on Si(100) and α-SiC(0001). Problems derived primarily from interface related defects and subboundaries in the material have prevented the optimization of the quality of the films. However, deposition on these materials oriented 2-4° off-axis allows the elimination of the APBs in the material grown on Si(100) and the DPBs in the material deposited on SiC(0001); the latter resulting combination of α-SiC on α-SiC appears especially viable for device fabrication. Despite the defects, the existence of the films has allowed substantial progress in the development and understanding of doping procedures both during growth and via ion implantation (at low and high temperatures), dopant activation, dry etching, electrical properties and device development. This collective research has shown that continued emphasis must be placed on improvement of the quality of the films.

ACKNOWLEDGEMENT

The authors enthusiastically acknowledge the support of this program by the Office of Naval Research under contract N00014-82-K-0182 P005. Appreciation is also expressed to Dr. S.P. Withrow for his assistance with the ion implantation research under U.S. D.O.E. Division of Materials Sciences contract D.E. - AC05-840 - R21400 with Martin Marietta Energy Systems, Inc.; P. Astell-Burt and P. Blackborow of Plasma Technology, Inc., for assistance with dry etching and to Dr. G. Carver of MBS and J. Wortman of NCSU for valuable discussions regarding device research.

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